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deliverable report

Summary of the SiEM project

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Abstract:

This report summarizes the development of a process for producing a Silicon Electron Multiplier (SiEM) demonstrator based on Deep Reactive Ion Etching (DRIE). This work was carried out under WP13 of the AIDAinnova project as a Blue-Sky R&D activity. The fabrication method, trials, and validation through simulation are described. The current status of demonstrator production, developed characterisation tools, and parallel alternative developments are presented. Challenges encountered are highlighted, and the most promising future directions are discussed.

AIDAinnova Consortium, 2025

For more information on AIDAinnova, its partners and contributors please see <http://aidainnova.web.cern.ch/>

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Delivery Slip

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**Executive summary**

*This deliverable presents the development and progress in making a demonstrator onovel Silicon Electron Multiplier (SiEM) sensor. It is pursued under the AIDAinnova WP13 Blue-Sky R&D framework. The SiEM concept aims to integrate a radiation-hard internal gain mechanism via metallic electrodes embedded in silicon, with the potential to achieve fine segmentation (<10 µm), high timing resolution (~50 ps), and improved radiation tolerance, positioning it as a strong candidate for next-generation tracking detectors.*

*The project began with extensive TCAD simulations to define the detector architecture and predict performance under realistic conditions. These studies informed the design of a simplified strip-based demonstrator capable of showcasing the gain mechanism. The fabrication process was centred around Deep Reactive Ion Etching (DRIE), with a focus on achieving optimal pillar geometries and electrode placement to generate the necessary electric fields for avalanche multiplication.*

*Significant R&D was conducted to tune the DRIE process. Early tests using laser photolithography reached a limit at 2 µm pillar tips, prompting adaptations to achieve narrower base widths. Despite slanted wall geometries, simulations confirmed gain retention, albeit requiring higher bias voltages. This was followed by the development of a robust metallisation process using metal etching, after lift-off methods proved unreliable, resulting in improved pattern fidelity and process repeatability.*

*The move to stepper photolithography enabled consistent wafer-scale fabrication, resolving planarity and resolution issues encountered with laser-based methods. Masks were designed for all process stages, and mechanical wafers were successfully produced with homogenous demonstrator structures. However, the final wafer production was delayed due to damage to the DRIE machine at CNM, with completion expected before summer 2025.*

*In parallel, a complete characterisation chain was developed at CERN, built around the OPTIMA board and its daughter board designed specifically for the SiEM demonstrators. The system has been validated using LGADs and is integrated into various setups, including β-source, TCT, and Timepix4 telescope environments, enabling precise measurement of signal gain, timing resolution, and charge collection efficiency.*

*An alternative fabrication route using Metal-Assisted Chemical Etching (MacEtch) was also investigated for its potential to produce high-aspect ratio features with sub-2 µm pitch. While promising in terms of structural resolution, the use of metallic catalyst as a multiplication electrode introduced high leakage currents, limiting gain studies. A follow-up iteration with dielectric isolation is planned.*

*The report concludes that while the SiEM demonstrator's full characterisation awaits final production, all foundational steps have been completed, and simulations predict the expected performance is achievable. Future tests will confirm the viability of the gain mechanism and guide decisions on further development of this innovative sensor technology.*

# Introduction

The development of precision silicon sensors is a key area of advancement in high-energy physics, particularly for the innermost tracking devices of future collider experiments. These require a timing resolution on the order of 50 ps, pixel pitches of 50 µm or bellow, and radiation tolerance up to 1016-17neq.cm-2. The Silicon Electron Multiplier (SiEM) is one such innovation. It integrates an internal gain mechanism via a metallic electrodes embedded in the silicon bulk. As described in [1], SiEM aims to provide higher radiation tolerance than existing gain sensors (e.g., LGADs), since the gain mechanism is inherently radiation-hard, while maintaining comparable timing performance. It also enables pixel pitches below 10 µm, a segmentation level difficult to achieve with other silicon sensor technologies.

In 2020–2021, conceptual foundations were established using TCAD simulations. The proposed device guides electrons generated by a minimum ionising particle (MIP) into a narrow silicon channel or pillar, where charge multiplication occurs through impact ionisation due to the high electric field created by biased electrodes. As illustrated in Figure 1, the electric field is generated by the difference of potential applied to the multiplication electrodes (in the two-electrode configuration), or between the multiplication electrode and the readout electrode (in the single electrode configuration). The motion of those multiplied charges then induces a signal on the readout electrode located at the top of the silicon pillar.

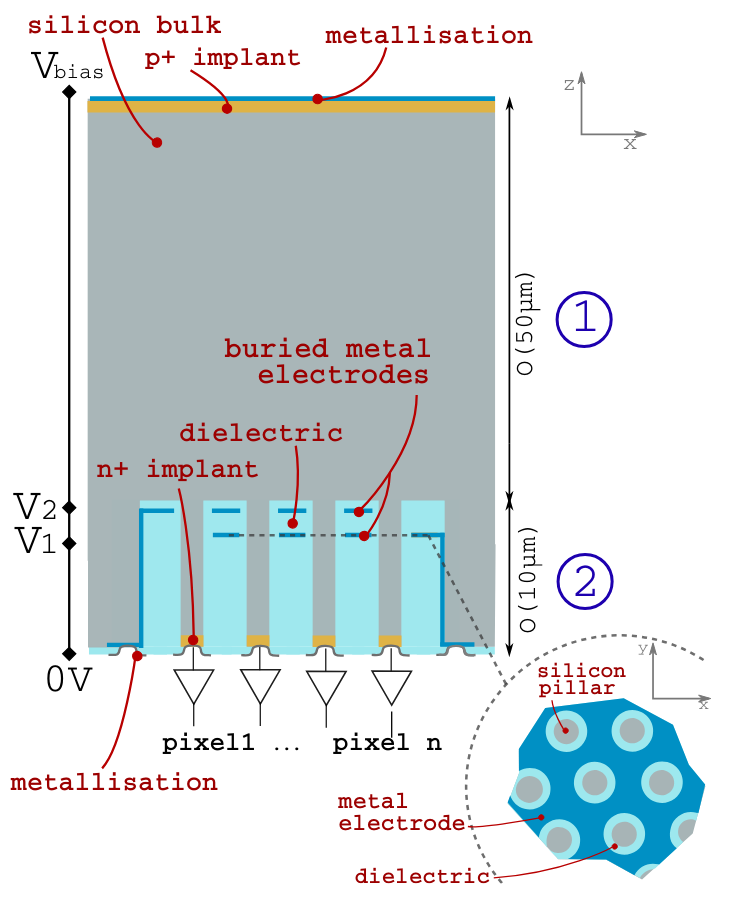


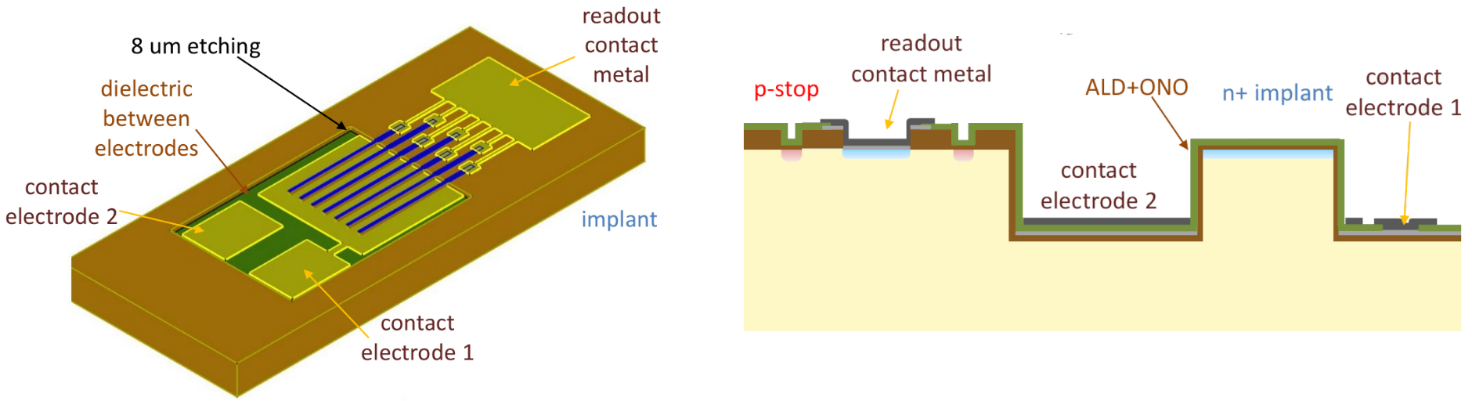
Figure 1: Schematic description of the SiEM detector. It consists of an O(50 μm) thick depleted silicon region 1 adjacent to a region 2 made of silicon pillars. In between the pillars two metallic electrodes, separated by a dielectric are buried. The electrodes produce a high electric field region in 2. As a particle passes through 1, primary electrons are produced by ionisation and drift toward 2 where they are multiplied and induce a signal while drifting towards the readout electrode. Taken from [1]

Building on this concept, the project was submitted to AIDAinnova's Blue-Sky R&D framework. The focus was on exploring the feasibility of fabricating such a sensor using a Deep Reactive Ion Etching (DRIE) based process. The study encompassed demonstrator design, production of test structure for etching and metallisation process development, the production of the demonstrator, as well as the preparation of characterisation tools and, once the demonstrator would be made available, the study of the demonstrator. Device simulations with Sentaurus TCAD informed key design decisions and guided development.

The project team includes CERN (simulation, characterisation) and CNM (fabrication, process definition, and test structure production).

# Design and process R&D

## Process description

Figure 2 : A 3D view of the demonstrator is shown on the left with the main element of the structure indicated. On the right a cross section of the various layers is shown.

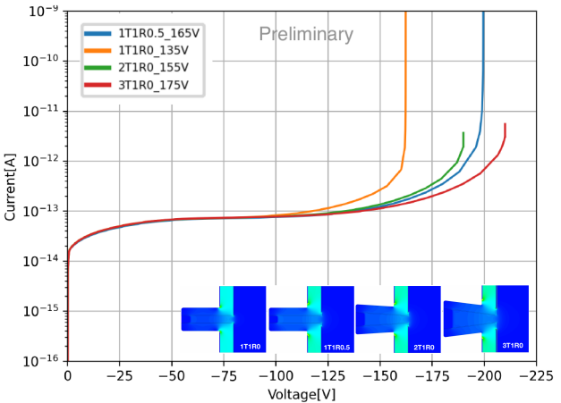
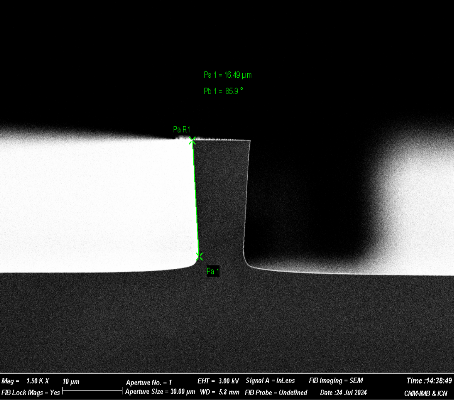
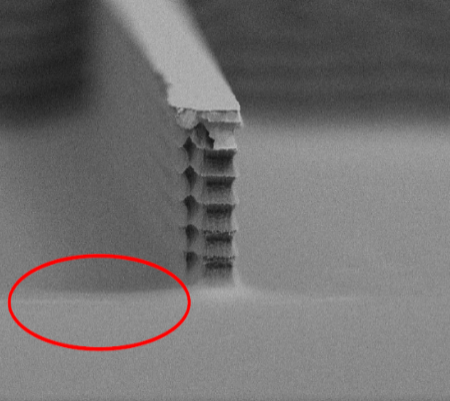
The design of the test structure, as well as the various steps of the process, were defined early in the project. To simplify the demonstrator geometry as much as possible, facilitate characterisation, and still allow for demonstration of the gain mechanism, it was decided to adopt a strip geometry, with seven strips interconnected on a single readout pad, as illustrated in Figure 2.

The production process is as follows: after the doping stage, the pillars are created by etching using DRIE process to a depth of 8 to 10 µm. Simulations showed that the smaller the width of the pillar, the better the signal amplification, with an optimal performance observed at a 1 µm width. This step is followed by atomic layer deposition of a dielectric, to separate the contact electrode from the silicon bulk. Subsequently, metallisation is performed to produce the first amplification electrode. A second dielectric layer is then deposited, followed by another metallisation step to create the second electrode and the readout electrode. Simulation also allowed to estimate the optimal thickness of the dielectric in between multiplication electrodes and verify that the proposed geometries and material maintained the expected performances.

## DRIE R&D

The tuning of the DRIE process was expected to require several iterations. To enable a fast development turnaround, it was decided to use laser photolithography. This method allows new patterns to be produced quickly and at low cost. However, due to the limited resolution of the laser, a 1 µm width could not be achieved at the tip of the strip pillars. Tests showed that pillar widths down to 2 µm could be reliably fabricated.

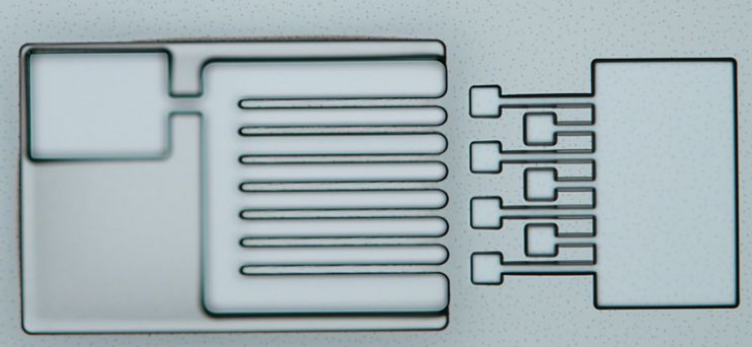
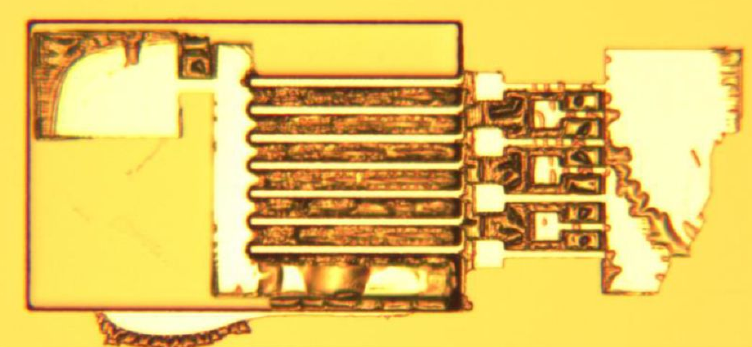
In conjunction with an etching profile producing walls angled at 85 degrees relative to the top surface of the pillar, a 1 µm width at the base of the pillar could be achieved. This wall angle results in a slight retraction of the metal electrode with respect to the pillar base. TCAD simulations demonstrated that the presence of slanted walls does not alter the gain mechanism; the resulting behaviour is equivalent to that of straight-wall pillars with retracted electrodes. As a consequence, the demonstrator needs to be operated at a higher voltage to achieve the desired gain, as illustrated in Figure 3.

Figure 3: first DRIE test were giving rough walls with large scallopping (left), after optimising the DRIE process, expected smootheness and wall angle were achieved (center). Simulated I-V characteristics shows that gain (visible with the slowly increasing current), can be achieved in both straight and slanted wall geometry, and that the electrode retraction drives the operating voltage.

## Metallisation R&D

Once the pillars were etched, a patterned metallisation needed to be created to serve as the amplification electrodes. The significant depth difference between the bottom and the tip of the pillars made this a non-trivial operation. In the first iteration, photoresist was deposited and exposed, followed by metal deposition via sputtering. A subsequent development step was intended to lift off the metal deposited on top of the exposed photoresist. However, this method resulted in poor pattern quality and significant inhomogeneity.

To address this, the process was revised: the metal layer was first deposited, followed by the application of photoresist. The photoresist was then selectively opened in the regions where the metal needed to be removed, and the exposed metal etched using reactive ion etching. This revised approach significantly improved patterning quality, as illustrated in Figure 4.

Figure 4: The first metallisation process on the left gave poor pattern quality after lift-off while on the new process is much more homogeneous.

# Production

## From laser to stepper photolithography

While laser photolithography offered flexibility during the prototyping phase, challenges arose when transitioning to full-wafer production, where the demonstrator fabrication needed to be repeated multiple times across the wafer surface. It became apparent that the wafer’s planarity was insufficient to maintain consistent laser focus and achieve uniform pattern quality across the entire surface. As a result, the production process was shifted to a stepper-based photolithography approach. Photomasks were designed and fabricated for the various process steps—including p- and n-type doping, DRIE, metallisation, and others—and are shown in Figure 5. Four mechanical wafers were produced to validate alignment, etching, and metallisation performance. If this modification of the overall process delayed the production compared to the original plans, the adoption of stepper lithography markedly improved feature resolution, overlay accuracy, and overall process yield.

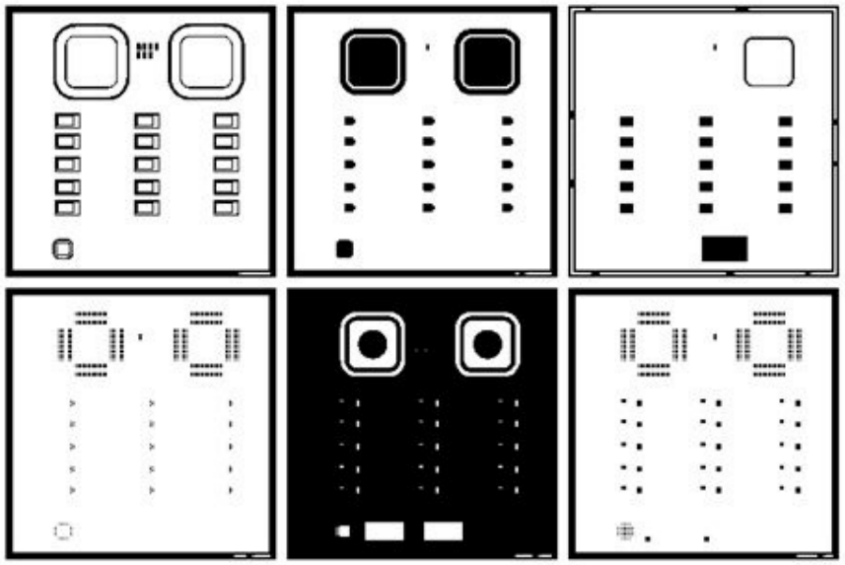


Figure 5: The mask used in stepper photolithography (left) and the mechanical wafer after the etching step (right). The demonstrators are visible over the whole surface and were shown to be homogeneously produced.

## STATUS of the final production

The p- and n-type doping of the production wafer was completed at the end of 2024. Unfortunately, at that point, the DRIE machine at CNM suffered damage and required repairs. Although the machine returned to operation at the end of April, a significant production backlog had accumulated in the meantime, delaying further processing. As a result, the fabrication of the SiEM demonstrator has not yet been finalised. It is currently expected to be processed before summer 2025.

# Characterisation tools

Once the production of the demonstrator is finalised, characterisation can begin. A board dedicated to the preamplification of signals generated in silicon sensor test structures has been designed as part of the CERN EP R&D WP1.1 program: the OPTIMA board [4]. A dedicated mezzanine for OPTIMA was specifically developed to test the CNM SiEM structures. The OPTIMA is read out using a SAMPIC digitiser. This system has been integrated into a β-source setup at CERN as well as a recently procured and commissioned TCT setup. Additionally, it has been incorporated into the TPX4 telescope at the SPS [3,5], as shown in Figure 6. This integration will enable precise measurements of gain, time resolution, and charge collection efficiency as a function of the impinging particle's position. The characterisation chain has already been validated on LGADs and is ready to receive the first SiEM demonstrators.

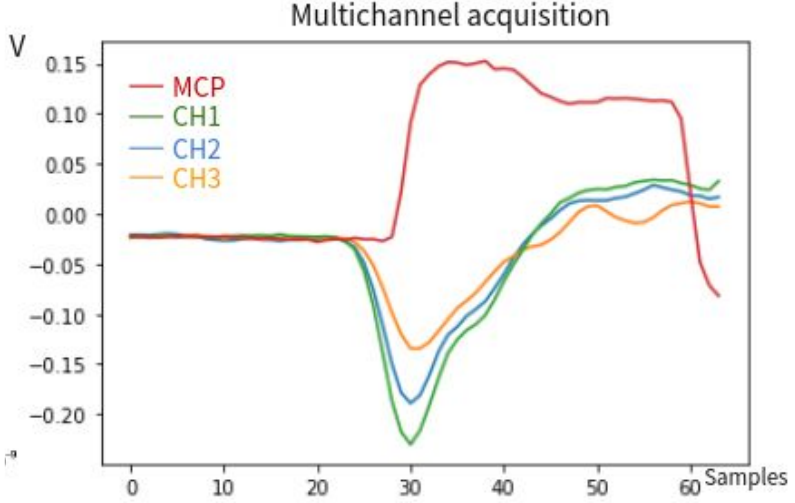
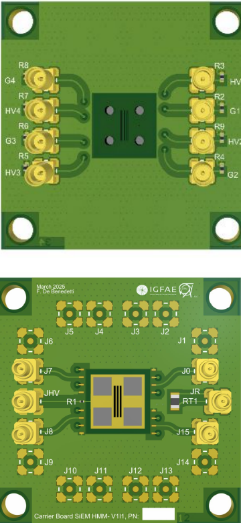
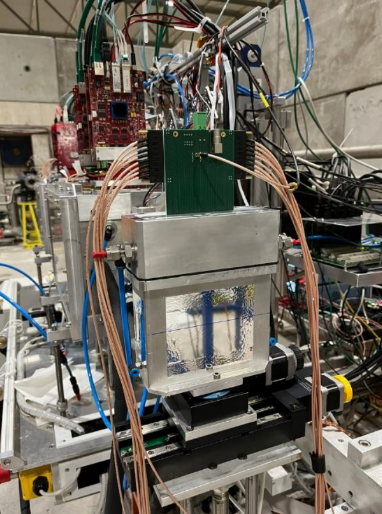


Figure 6: The OPTIMA board in its cold box on the backstage of the Timepix4 telescope at the SPS (left). The OPTIMA daughter board dedicated to host the SiEM demonstrator (center) Waveform of LGADs registered through the OPTIMA+SAMPIC, with signals from the MCP used for fast timing reference (right)

# ALTERNATIVE technology

In parallel with the primary DRIE-based approach, an alternative fabrication route using Metal-Assisted Chemical Etching (MacEtch) was explored for its potential to produce cost-effective structures with very high aspect ratios. In this method, a patterned metal layer catalyses the etching process. Although MacEtch is not commonly employed in sensor fabrication, it presents new possibilities, and one of the aims of this study was to verify whether the pn-junction properties of the etched sensor could be preserved. Test structures were fabricated and IV characteristics measured, confirming that the MacEtch process does indeed maintain diode behaviour.

The results in terms of pillar morphology were extremely promising, with pitches below 2 µm and pillar heights in the 10–20 µm range, which is optimal in a single electrode SiEM configuration. However, the use of the metal catalyst as a multiplication electrode resulted in the formation of a Schottky junction, leading to large leakage currents that complicate the testing of the amplification properties. These results are detailed in [2]. A second production run is planned in which a dielectric layer will be introduced between the catalyst and the amplification electrode to address this issue.

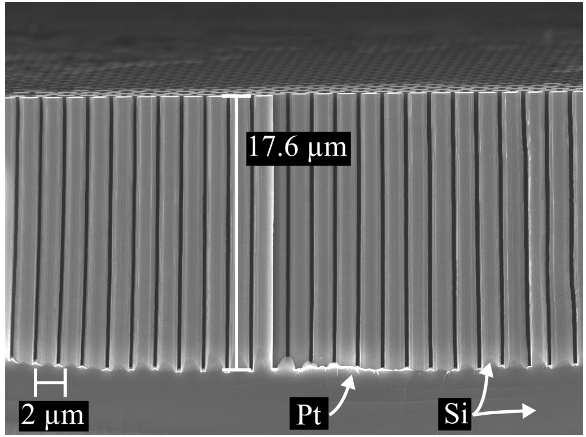
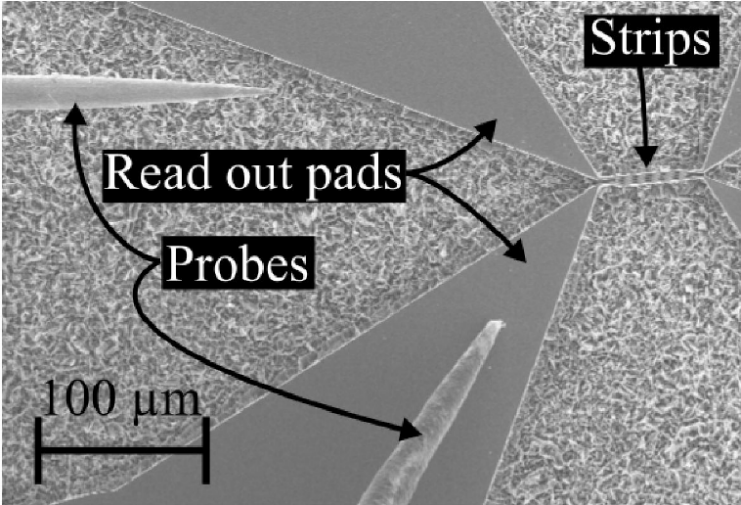


Figure 7: (left) View of the strip version of the MacEtch structure. The probes used to measure the IV characteristics reported in [2] are visible. (right) details of the pixel pillars is shown. The platinium (Pt) was used both to catalyse the etching and as amplification electrode.

# FUTURE PLANS / Conclusion / relation to other AIDA-2020 work

Over the course of the project, the feasibility of fabricating a silicon electron multiplier (SiEM) using a deep reactive ion etching (DRIE)-based process has been successfully demonstrated. The process steps were thoroughly studied and adapted, and device simulations were aligned accordingly. Although the final demonstrator production was delayed due to the temporary unavailability of the DRIE machine, it is expected to be completed before the end of summer 2025. In parallel, the characterisation tools have been fully developed and commissioned, ensuring that the gain mechanism can be promptly studied once the demonstrator is available.

Alternative processing methods—particularly those based on metal-assisted chemical etching—have also been investigated and yielded promising preliminary results. These will be followed up with a second production run aimed at overcoming the high-current limitation observed in initial tests. In the coming months, both the demonstrator developed in this project and a separate demonstrator produced by another vendor will undergo testing. The results of these qualification campaigns will be critical in assessing whether the SiEM technology can deliver the expected performance and in determining whether further development should be pursued.

In conclusion, while a definitive answer on whether gain can be achieved with embedded metallic electrodes awaits the final demonstrator, the construction feasibility of a silicon electron multiplier has been clearly demonstrated. Simulations indicate that the same performance levels can be achieved when accounting for the constraints imposed by a realistic fabrication process.

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# Annex: Glossary

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| --- | --- |
| Acronym | Definition |
| DRIE | Deep reactive ion etching |
| MACETCH | Metal assisted chemical etching |
| TPX4 | Timepix 4 |